Intel® 31244 PCI-X to Serial ATA Controller

Design Layout Review Checklist

October 2002

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Revision History

Date	Revision	Description
October 2002	001	Initial Release.

1.0 Electrical Design/Layout Review Checklist

This checklist is for the Intel® 31244 PCI-X to Serial ATA controller (31244).

Table 1. Electrical Design/Layout Review Checklist (Sheet 1 of 3)

Rule or Guideline	Compliance	
	Yes	No
PCI-X System Electrical Checklist		
Characteristic impedance of signal traces is 60 W ±10%.		
Signal propagation delay of traces is between 150 and 190 ps/inch, inclusive. (Same as conventional PCI.)		
When the source bridge requires **IDSEL** inputs to be resistively coupled to **AD** bits, those resistors have a value of a least 2 KΩ XME10.		
When the source bridge requires **IDSEL** inputs to be resistively coupled to **AD** bits, devices 1-4 connect to **AD[17]** through **AD[20]** respectively XME11.		
When the system includes slots for add-in cards, the system provides a circuit for sensing the connection of the **PCIXCAP** pin of all add-in cards XME12. Note: on add-in card not on the 31244.		
PCIXCAP pin is connected to ground through a 0.01 µF ±10% capacitor for PCI-X 133, or through a 10 K ±5% resistor in parallel with a 0.01 mF ±10% capacitor for PCI-X 66 XME13. Note: on add-in card not on 31244.		
PCIXCAP - The maximum trace length between the resistor (when installed), capacitor, and connector contact is 0.25 inches. The maximum trace length between the resistor (when installed), capacitor, and ground is 0.1 inch. A PCI-X card is not permitted to connect **PCIXCAP** to anything else including supply voltages and device input and output pins.		
PRSNT[1:2]# are connected to show correct power consumption. EE1. **NOTE:** on add-in card not on 31244. One of the present pins PRSNT1 or PRSNT2 on a PCI add-in card must be tied to GND to signal to the motherboard there is a card present in slot.		
The PCI edge finger matches the connector pinout specification.		
All GND fingers are provided and are bussed together.		
All bussed signals contain no more than ONE 10 pF (maximum) load. EE8.		
M66EN finger (pin 49, side B) is either an input or a no-connect. EE9.		
PCI connector pins: Ensure 3.3 V pins (even when they are not actually delivering power) and any unused 5 V and V_{IO} pins on the PCI edge connector provide an AC return path. These pins must have plated edge fingers and be decoupled to the ground plane, on the add-in board, to ensure they continue to function as efficient AC reference points.		
All RESERVED fingers are no-connect and are NOT bussed together. EE13.		
Add-in card protection circuitry (zener diode) on INTA#, to prevent chip damage when card plugged into a 5 V slot.		
Add-in card trace length for **AD[31::0]** is between 0.75 inches and 1.5 inches, inclusive.		
Add-in card trace length for **AD[63::32]** is between 1.75 inches and 2.75 inches, inclusive.		
Add-in card trace length for **RST#** is between 0.75 inches and 3.0 inches, inclusive.		
PCI Clock Trace length for **P_CLK** is between 2.4 inches and 2.6 inches, inclusive and routes only to one load for add-in card. (Same as conventional PCI.) Total length for non-add-in card is < 8 inches.		
PCI Clock Buffer: **P_CLK** lengths are matched to 0.1 inch.		
PCI Clock Buffer: use low skew clock buffer.		
PCI Clock Buffer: **P_CLK** lines at least 25 mils from each other and themselves.		
PCI Address Bus **AD**: wiring lengths follow recommendations in the *Intel® 31244 PCI-X to Serial ATA Controller Design Guide*, dependent on speed and number of slots.		
P_SERR#, P_TRDY#, P_LOCK#, P_PERR#, P_DEVSEL#, P_FRAME#, P_STOP#, P_IRDY#, P_INTA#, P_AD[63:32], P_C/BE[7:4]#, P_PAR64, P_REQ64# and P_ACK64# use appropriate pull-up resistor (10 K acceptable).		
32BITPCI# 1 K pull-up for 64-bit controls status bit 16, in the PCI-X Status Register. When pulled down, reports a 0, for a 32-bit bus. When pulled up, reports 1, a 64-bit device.		
CAP2 This pin is connected to a 0.015 µF cap with the other end connected to the CAP3 pin.		
CAP3 This pin is connected to a 0.015 µF cap with the other end connected to the CAP2 pin.		

Table 1. Electrical Design/Layout Review Checklist (Sheet 2 of 3)

Rule or Guideline	Compliance	
	Yes	No
SATA Interface		
SATA Clock Buffer: When using a clock buffer for a multiple 31244 design, **SATA CLKIN line** lengths going to each of the 31244 chip CLKIN pins are matched to 0.1 inch.		
SATA Clock Buffer: use low skew clock buffer.		
SATA Clock Buffer: **CLKIN** lines at least 25 mils from each other and themselves.		
TX0P, TX0N, TX1P, TX1N,TX2P,TX2N, **RX0P, RX0N, RX1P, RX1N, RX2P, RX2N** must have a series 0.01 µF capacitor.		
DPA_MODE# GND to enable DPA Mode, 1 K pull-up to enable Legacy Mode.		
CAP0: This pin is connected to a 0.1 µF cap with the other end connected to the CAP1 pin.		
CAP1: This pin is connected to a 0.1 µF cap with the other end connected to the CAP0 pin.		
SATA Normal Voltage Mode (see section 5.1 in *Intel® 31244 PCI-X to Serial ATA Controller Design Guide*)		
Single-Ended Trace Impedance: Microstrip stackup with reference plane as ground.		
Impedance: 100Ω differential impedance.		
Trace Thickness: 1.4 mil.		
Trace Width: 5 mil.		
Intra Pair Trace Spacing: 7 mil.		
Pair to Pair Trace Spacing: 20 mil minimum.		
Trace Length: 2 inches to 5 inches.		
Trace Length Matching: 100 mils.		
Vias: Minimize number of vias (none preferred). Each channel in the pair has an equal number of vias.		
SATA Extended Voltage Mode: Motherboard Parameters (see section 5.2.2 in *Intel® 31244 PCI-X to Serial ATA Controller Design Guide*)		
Microstrip Stackup: refer to the *Intel® 31244 PCI-X to Serial ATA Controller Design Guide* for more details.		
Single-Ended Trace Impedance: 55Ω +/- 12%. Reference plane is GND.		
Differential Trace Impedance: 100Ω +/- 15%.		
Trace Thickness: 1.4 mil.		
Trace Width: 5 mil.		
Intra Pair Trace Spacing: 15 mil intra-pair to pair center - to - center.		
Pair-to-Pair Trace Spacing: 55 mil pair to pair center - to - center.		
Trace Length: 2 inches to 6 inches.		
Trace Length Matching: 10 mil Intra-pair matching.		
Vias 0: Minimize number of vias (none preferred). Each channel in the pair has an equal number of vias.		
SATA Extended Voltage Mode: Backplane Stripline Stackup (see section 5.2.3 in *Intel® 31244 PCI-X to Serial ATA Controller Design Guide*)		
Differential impedance: 100Ω +/- 15%		
Single Ended Trace Impedance: 60Ω +/- 14%. Reference Plane ground.		
Trace Thickness: 1.4 mil.		
Trace Width: 11.5 mil.		
Intra Pair Trace Spacing: 29.7 mil intra-pair center-to-center (broadside coupled).		
Pair to Pair Trace Spacing: 60 mil pair-to-pair, center-to-center for two adjacent differential pairs.		
Trace Length: 2 inches to 14 inches.		
Trace Length Matching: 10 mils intra-pair matching.		
R1: 15Ω +/- 5%. Required only for write topology, see *Intel® 31244 PCI-X to Serial ATA Controller Design Guide*, Figure 14,		
R2: 150Ω +/- 5%. Required only for write topology, see *Intel® 31244 PCI-X to Serial ATA Controller Design Guide*, Figure 14.		

Table 1. Electrical Design/Layout Review Checklist (Sheet 3 of 3)

Rule or Guideline	Compliance	
	Yes	No
Miscellaneous Signals		
TEST0: Connect to GND.		
TOUT: NC.		
SSCEN: 1 K Pull-up to enable GND to disable Spread Spectrum Clocking.		
TRST#: GND when not used.		
RBIAS: Connect pin to a 1% 1000Ω resistor to GND.		
Voltage Signals		
V18A: Connect this pin to 10 µF capacitor and 0.1 µF cap in V18A comments parallel. The opposite end of the caps are connected to GND.		
V18B: Connect this pin to 10 µF capacitor and 0.1 µF cap in parallel. The opposite end of the caps are connected to GND.		
VA0 (Refer to Figure 1): The 22 µF bulk capacitors must be low ESR solid tantalum and the 0.1 µF ceramic capacitor must be of the type X7R. The node connecting VA0 and VA1, must be as short as possible.		
VA1 (Refer to Figure 1): The 22 µF bulk capacitors must be low ESR solid tantalum and the 0.1 µF ceramic capacitor must be of the type X7R. The node connecting VA0 and VA1, must be as short as possible.		
V_{SS}: Ground		
V_{CC}: 2.5 V Digital Logic Power Supply.		
V_{IO}: 3.3 V PCI I/O Power Supply.		
V_{CC0}, V_{CC1}, V_{CC2}, V_{CC3}: 2.5 V High-Speed I/O Power Supply for each SATA channel.		
V_{CC5REF}: In 5 V tolerant systems, this is connected to a 5 V supply. In 3.3 V powered systems this is connected to a 3.3 V. In PCI add-in cards, this is connected to I/O Power (10 A, 16 A, 19 B, 59 A and 59 B).		
General Decoupling		
The decoupling must average at least 0.01 µF (high-speed) per V_{CC} pin.		
The trace length from pin pad to capacitor pad is no greater than 0.25 inches using a trace width of at least 0.02 inches.		
Add one high-frequency decoupling capacitor per power pin where possible. To minimize inductance, use 0805 or 1206 style surface-mount 0.01 µF or 0.1 µf capacitors.		
General Note		
All unused inputs on any chips are connected to GND		

Figure 1. Intel® 31244 PCI-X to Serial ATA Controller Block Diagram